

FEATURES

- 8th Order, Linear Phase Filter in SO-8 Package
- Raised Cosine Amplitude Response
- -43dB Attenuation at $2 \times f_{\text{CUTOFF}}$
- Wideband Noise: $140\mu\text{V}_{\text{RMS}}$
- Operates from Single 5V Supply to $\pm 5\text{V}$ Power Supplies
- Clock-Tunable to 200kHz with $\pm 5\text{V}$ Supplies
- Clock-Tunable to 120kHz with Single 5V Supply

APPLICATIONS

- Digital Communication Filter
- Antialiasing Filter with Linear Phase
- Smoothing Filters

DESCRIPTION

The LTC[®]1069-7 is a monolithic, clock-tunable, linear phase, 8th order lowpass filter. The amplitude response of the filter approximates a raised cosine filter with an alpha of one. The gain at the cutoff frequency is -3dB and the attenuation at twice the cutoff frequency is 43dB . The


cutoff frequency of the LTC1069-7 is set by an external clock and is equal to the clock frequency divided by 25. The ratio of the internal sampling frequency to the cutoff frequency is 50:1 that is, the input signal is sampled twice per clock cycle to lower the risk of aliasing. The LTC1069-7 can be operated from a single 5V supply up to dual $\pm 5\text{V}$ supplies.

The gain and phase response of the LTC1069-7 can be used in digital communication systems where pulse shaping and channel bandwidth limiting must be carried out. Any system that requires an analog filter with linear phase and sharper roll off than conventional Bessel filters can use the LTC1069-7.

The LTC1069-7 has a wide dynamic range. With $\pm 5\text{V}$ supplies and an input range of 0.1V_{RMS} to 2V_{RMS} , the signal-to-(noise + THD) ratio is $\geq 60\text{dB}$. The wideband noise of the LTC1069-7 is $140\mu\text{V}_{\text{RMS}}$. *Unlike other LTC1069-X filters, the typical passband gain of the LTC1069-7 is equal to -1V/V .*

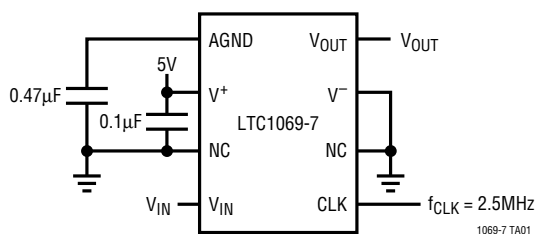
The LTC1069-7 is available in an SO-8 package.

Other filter responses with lower power/speed specifications can be obtained. Please contact LTC Marketing.

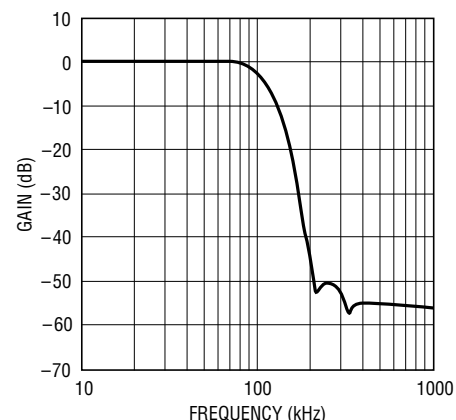
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TYPICAL APPLICATION

Single 5V Supply, Linear Phase 100kHz Lowpass Filter



Frequency Response

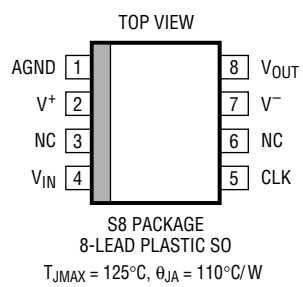


1069-7 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 12V
 Power Dissipation 400mW
 Operating Temperature Range
 LTC1069-7C 0°C to 70°C
 LTC1069-7I -40°C to 85°C
 Storage Temperature -65°C to 150°C
 Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

 <p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 110^{\circ}C/W$</p>	ORDER PART NUMBER
	LTC1069-7CS8 LTC1069-7IS8
	S8 PART MARKING
	10697 10697I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

f_{CUTOFF} is the filter's cutoff frequency and is equal to $f_{CLK}/25$. The f_{CLK} signal level is TTL or CMOS (max clock rise or fall time $\leq 1\mu s$), $R_L = 10k$, $T_A = 25^{\circ}C$, unless otherwise specified. All AC gains are measured relative to the passband gain.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Passband Gain ($f_{IN} \leq 0.2f_{CUTOFF}$)	$V_S = \pm 5V, f_{CLK} = 2.5MHz$ $f_{TEST} = 1kHz, V_{IN} = 1V_{RMS}$	●	-0.10	± 0.75 ± 0.90	dB dB
	$V_S = 4.75V, f_{CLK} = 500kHz$ $f_{TEST} = 1kHz, V_{IN} = 0.5V_{RMS}$	●	-0.10	± 0.75 ± 0.90	dB dB
Gain at $0.25f_{CUTOFF}$	$V_S = \pm 5V, f_{CLK} = 2.5MHz$ $f_{TEST} = 25kHz, V_{IN} = 1V_{RMS}$	●	-0.30	-0.1	dB dB
	$V_S = 4.75V, f_{CLK} = 500kHz$ $f_{TEST} = 5kHz, V_{IN} = 0.5V_{RMS}$	●	-0.30	0.15	dB dB
Gain at $0.50f_{CUTOFF}$	$V_S = \pm 5V, f_{CLK} = 2.5MHz$ $f_{TEST} = 50kHz, V_{IN} = 1V_{RMS}$	●	-1.0	-0.35	dB dB
	$V_S = 4.75V, f_{CLK} = 500kHz$ $f_{TEST} = 10kHz, V_{IN} = 0.5V_{RMS}$	●	-0.30	0	dB dB
Gain at $0.75f_{CUTOFF}$	$V_S = \pm 5V, f_{CLK} = 2.5MHz$ $f_{TEST} = 75kHz, V_{IN} = 1V_{RMS}$	●	-1.65	-0.80	dB dB
	$V_S = 4.75V, f_{CLK} = 500kHz$ $f_{TEST} = 15kHz, V_{IN} = 0.5V_{RMS}$	●	-0.75	-0.25	dB dB
Gain at f_{CUTOFF}	$V_S = \pm 5V, f_{CLK} = 2.5MHz$ $f_{TEST} = 100kHz, V_{IN} = 1V_{RMS}$	●	-3.5	-2.7	dB dB
	$V_S = 4.75V, f_{CLK} = 500kHz$ $f_{TEST} = 20kHz, V_{IN} = 0.5V_{RMS}$	●	-2.9	-2.4	dB dB
Gain at $1.5f_{CUTOFF}$	$V_S = \pm 5V, f_{CLK} = 2.5MHz$ $f_{TEST} = 150kHz, V_{IN} = 1V_{RMS}$	●	-16.5	-14	dB dB
	$V_S = 4.75V, f_{CLK} = 500kHz$ $f_{TEST} = 30kHz, V_{IN} = 0.5V_{RMS}$	●	-18.1	-17	dB dB
Gain at $2.0f_{CUTOFF}$	$V_S = \pm 5V, f_{CLK} = 2.5MHz$ $f_{TEST} = 200kHz, V_{IN} = 1V_{RMS}$	●	-43	-38	dB dB
	$V_S = 4.75V, f_{CLK} = 500kHz$ $f_{TEST} = 40kHz, V_{IN} = 0.5V_{RMS}$	●	-41	-39	dB dB

ELECTRICAL CHARACTERISTICS

f_{CUTOFF} is the filter's cutoff frequency and is equal to $f_{CLK}/25$. The f_{CLK} signal level is TTL or CMOS (max clock rise or fall time $\leq 1\mu s$), $R_L = 10k$, $T_A = 25^\circ C$, unless otherwise specified. All AC gains are measured relative to the passband gain.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gain at $5.0f_{CUTOFF}$	$V_S = 4.75V$, $f_{CLK} = 500kHz$ $f_{TEST} = 100kHz$, $V_{IN} = 0.5V_{RMS}$	-70	-59	-55	dB
Gain at f_{CUTOFF} (160kHz)	$V_S = \pm 5V$, $f_{CLK} = 4MHz$ $f_{TEST} = 160kHz$, $V_{IN} = 1V_{RMS}$		-2.1		dB
Phase at $0.5f_{CUTOFF}$	$V_S = \pm 5V$, $f_{CLK} = 2.5MHz$ $f_{TEST} = 50kHz$	-35	-30.5	-25	Deg
Phase at f_{CUTOFF}	$V_S = \pm 5V$, $f_{CLK} = 2.5MHz$ $f_{TEST} = 100kHz$	-240	-235	-230	Deg
Passband Phase Deviation from Linear Phase (Note 1)	$V_S = \pm 5V$, $f_{CLK} = 500kHz$		-3.0		Deg
Output DC Offset (Input at GND)	$V_S = \pm 5V$, $f_{CLK} = 500kHz$ $V_S = 4.75V$, $f_{CLK} = 400kHz$		50 25	125	mV mV
Output Voltage Swing	$V_S = \pm 5V$, $I_{SOURCE}/I_{SINK} \leq 1mA$, $R_L = 10k$ $V_S = 4.75V$, $I_{SOURCE}/I_{SINK} \leq 1mA$, $R_L = 10k$	● ●	± 3.5 2.6	± 4.0 3.6	V V_{P-P}
Power Supply Current	$V_S = \pm 5V$, $f_{CLK} = 500kHz$	●		18 29	mA mA
	$V_S = 4.75V$, $f_{CLK} = 400kHz$	●		13 16.5	mA mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Phase Deviation = $1/2(\text{Phase at } 0Hz - \text{Phase at } f_{CUTOFF}) - (\text{Phase at } 0Hz - \text{Phase at } 0.5f_{CUTOFF})$

Phase at $0Hz = 180^\circ$ (guaranteed by design)

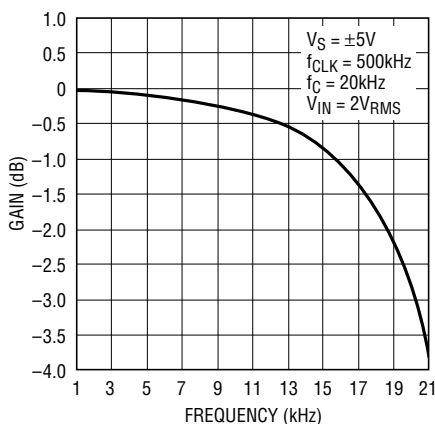
Example: An LTC1069-7 has Phase at $0.5f_{CUTOFF} = -30.5^\circ$ and Phase at $f_{CUTOFF} = -235^\circ$.

Passband Phase Deviation from Linear Phase

$$= 1/2[180^\circ - (-235^\circ)] - [(180^\circ - (-30.5^\circ))] = -3^\circ$$

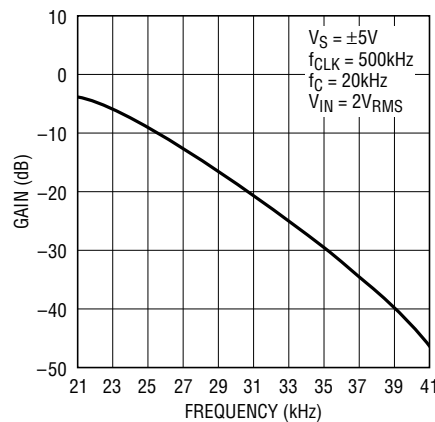
TYPICAL PERFORMANCE CHARACTERISTICS

Passband Gain vs Frequency



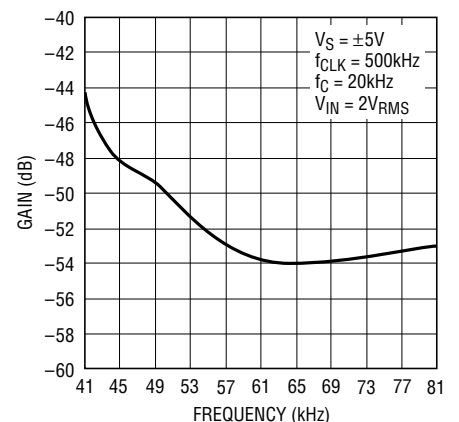
LTC1069-7 • TPC01

Transition Band Gain vs Frequency



LTC1069-7 • TPC02

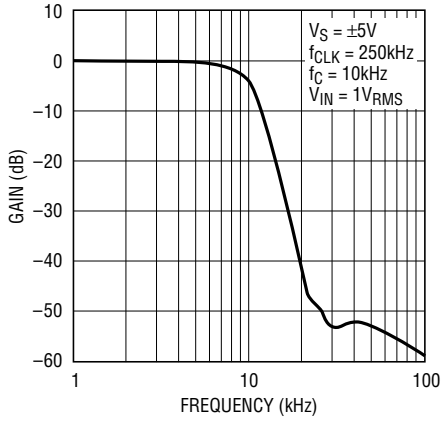
Stopband Gain vs Frequency



LTC1069-7 • TPC03

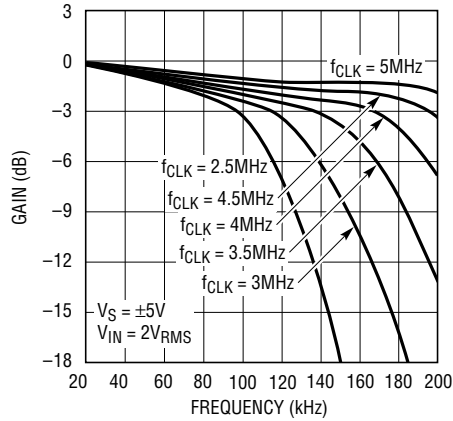
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency



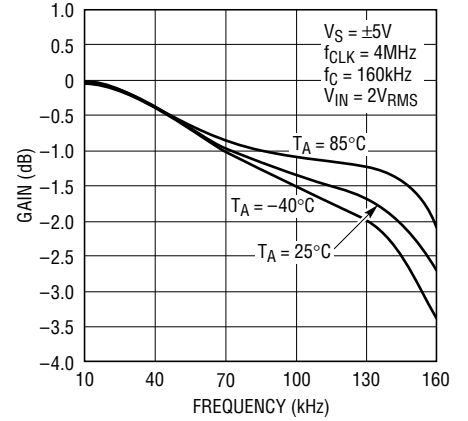
LTC1069-7 • TPC04

Passband Gain vs Clock Frequency



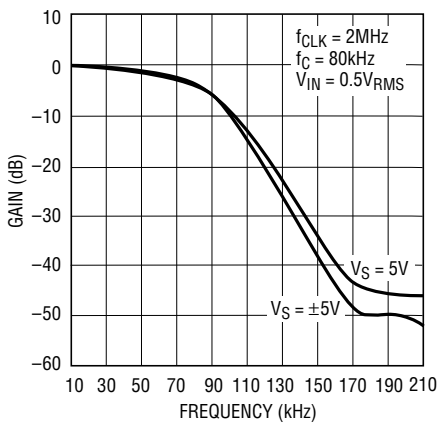
LTC1069-7 • TPC05

Passband Gain vs Frequency



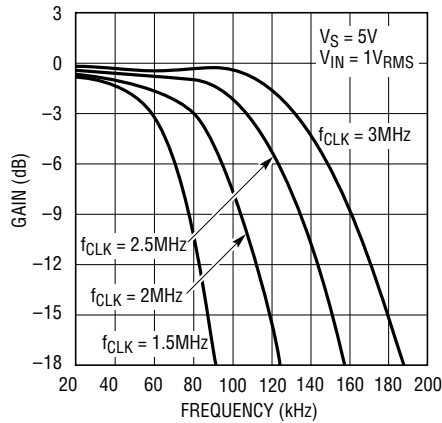
LTC1069-7 • TPC06

Gain vs Supply Voltage



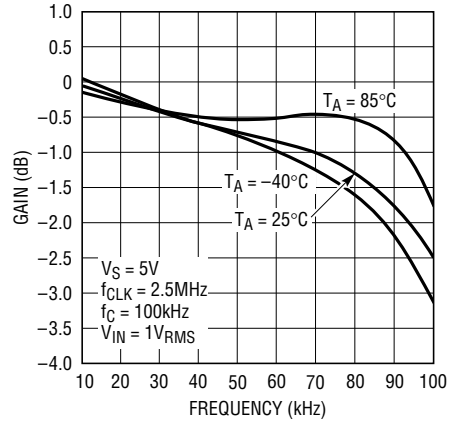
LTC1069-7 • TPC07

Passband Gain vs Clock Frequency



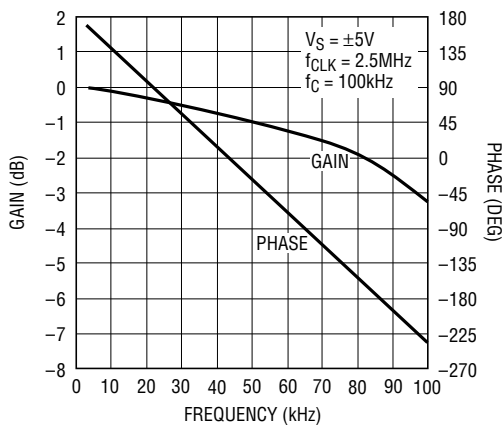
LTC1069-7 • TPC08

Passband Gain vs Frequency



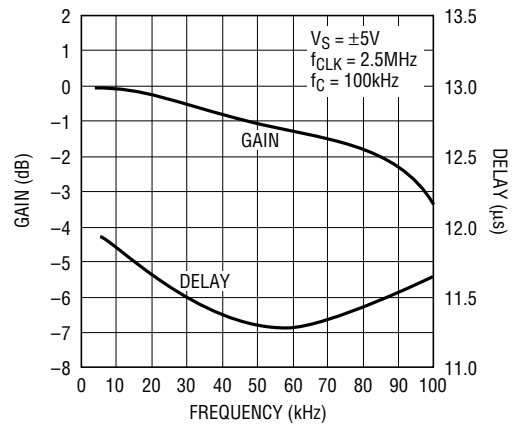
LTC1069-7 • TPC09

Passband Gain and Phase vs Frequency



LTC1069-7 • TPC10

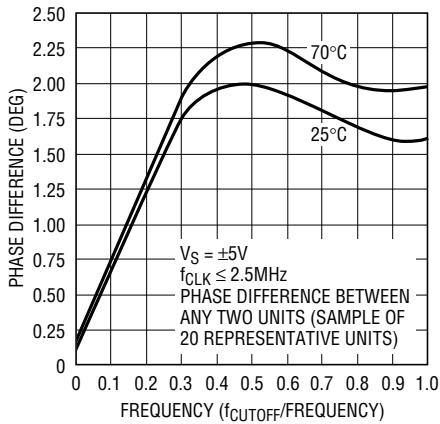
Passband Gain and Delay vs Frequency



LTC1069-7 • TPC12

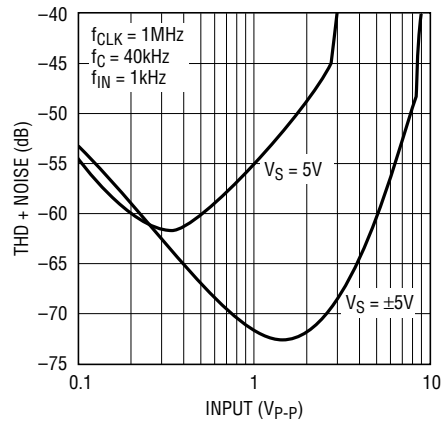
TYPICAL PERFORMANCE CHARACTERISTICS

Phase Matching vs Frequency



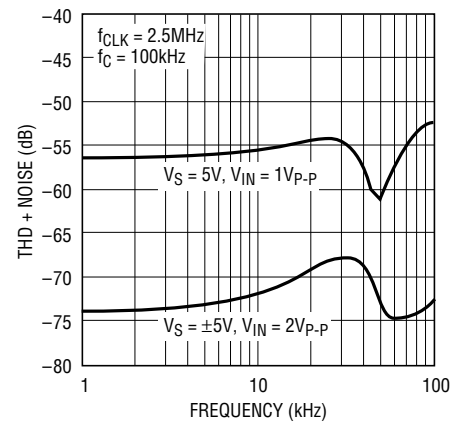
LTC1069-7 • TPC11

THD + Noise vs Input (V_{P-P})



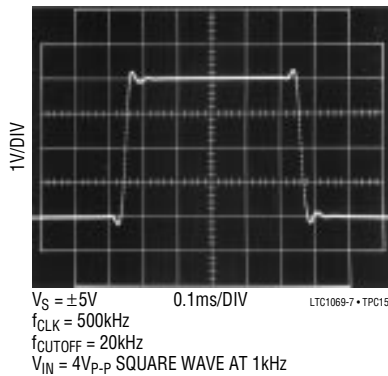
LTC1069-7 • TPC13

THD + Noise vs Frequency



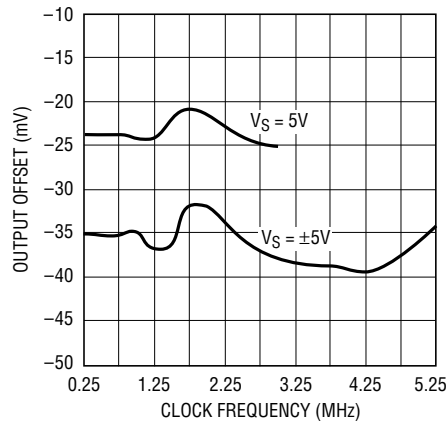
LTC1069-7 • TPC14

Transient Response



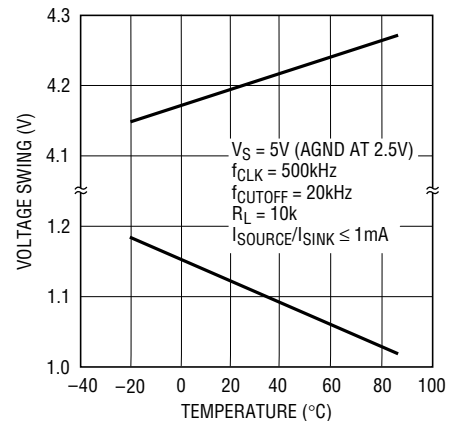
LTC1069-7 • TPC15

Output Offset vs Clock Frequency



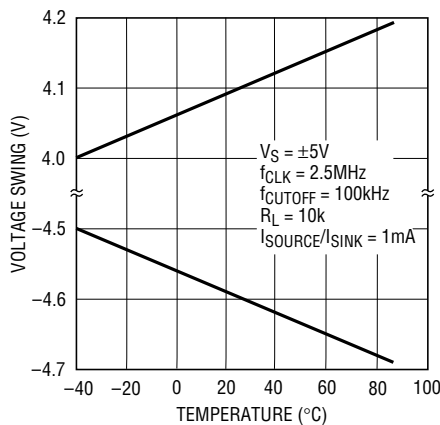
LTC1069-7 • TPC16

Output Voltage Swing vs Temperature



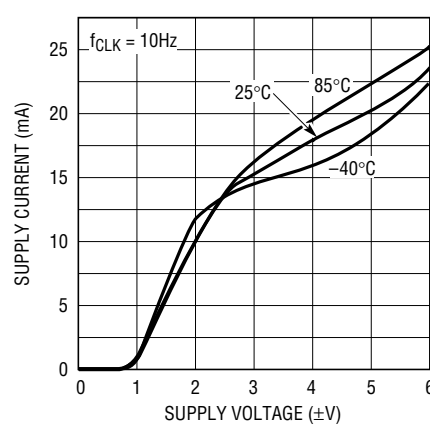
LTC1069-7 • TPC17

Output Voltage Swing vs Temperature



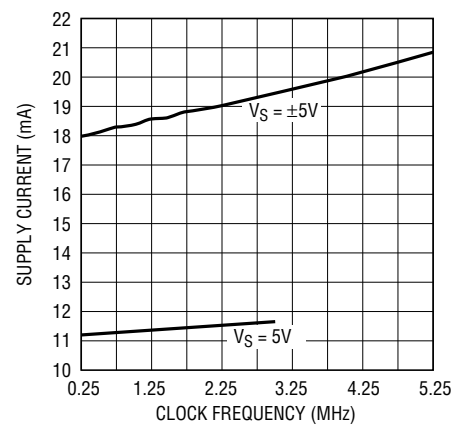
LTC1069-7 • TPC18

Supply Current vs Supply Voltage



LTC1069-7 • TPC19

Supply Current vs Clock Frequency



LTC1263 • TPC20

PIN FUNCTIONS

AGND (Pin 1): Analog Ground. The quality of the analog signal ground can affect the filter performance. For either single or dual supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, Pin 1 should be connected to the analog ground plane.

For single supply operation, Pin 1 should be bypassed to the analog ground plane with a capacitor $0.47\mu\text{F}$ or larger. An internal resistive divider biases Pin 1 to half the total power supply. Pin 1 should be buffered if used to bias other ICs. Figure 1 shows the connections for single supply operation.

V⁺, V⁻ (Pins 2, 7): Power Supplies. The V⁺ (Pin 2) and V⁻ (Pin 7) should be bypassed with a $0.1\mu\text{F}$ capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using switching power supplies will lower the signal-to-noise ratio of the filter. Unlike previous monolithic filters, the power supplies can be applied in any order, that is, the positive supply can be applied before the negative supply and vice versa. Figure 2 shows the connections for dual supply operation.

NC (Pins 3, 6): No Connection. Pins 3 and 6 are not connected to any internal circuitry; they should be tied to ground.

V_{IN} (Pin 4): Filter Input. The filter input pin is internally connected to the inverting inputs of two op amps through

a 36k resistor for each op amp. This parallel combination creates an 18k input impedance.

CLK (Pin 5): Clock Input. Any TTL or CMOS clock source with a square wave output and 50% duty cycle ($\pm 10\%$) is an adequate clock source for the device. The power supply for the clock source should not necessarily be the filter's power supply. The analog ground of the filter should only be connected to the clock's ground at a single point. Table 1 shows the clock's low and high level threshold value for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level on-time is greater than $0.42\mu\text{s}$ ($V_S = \pm 5\text{V}$). Sine waves less than 100kHz are not recommended for clock sources because excessive slow clock rise or fall times generate internal clock jitter. The maximum clock rise or fall time is $1\mu\text{s}$. The clock signal should be routed from the right side of the IC package to avoid coupling into any input or output analog signal path. A 1k resistor between the clock source and the clock input (Pin 5) will slow down the rise and fall times of the clock to further reduce charge coupling, Figure 1.

Table 1. Clock Source High and Low Thresholds

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = $\pm 5\text{V}$	1.5V	0.5V
Single Supply = 10V	6.5V	5.5V
Single Supply = 5V	1.5V	0.5V

V_{OUT} (Pin 8): Filter Output. Pin 8 is the output of the filter, and it can source 23mA or sink 16mA . The total harmonic distortion of the filter will degrade when driving coaxial cables or loads less than 20k without an output buffer.

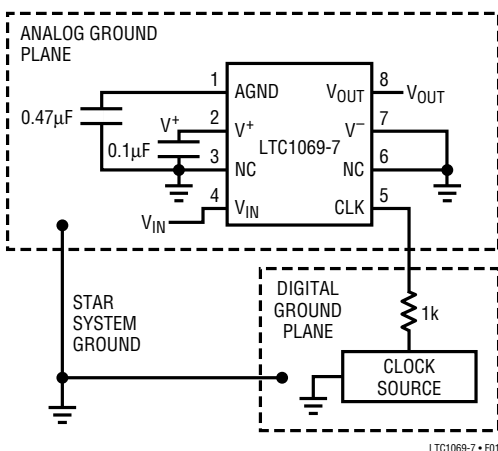


Figure 1. Connections for Single Supply Operation

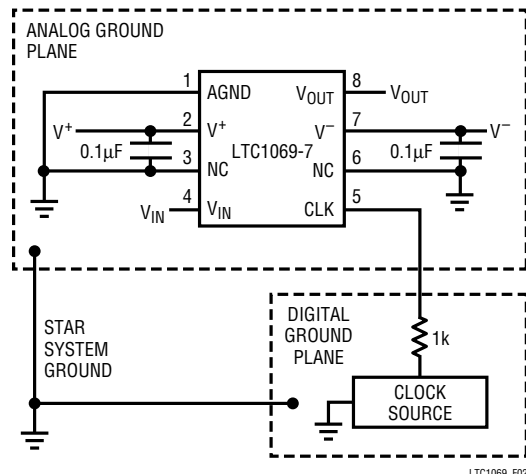


Figure 2. Connections for Dual Supply Operation

APPLICATIONS INFORMATION

Temperature Behavior

The power supply current of the LTC1069-7 has a positive temperature coefficient. The GBW product of its internal op amps is nearly constant and the speed of the device does not degrade at high temperatures.

Clock Feedthrough

The clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output (Pin 8). The clock feedthrough is tested with the input (Pin 4) shorted to the AGND pin and depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown on Table 2.

Table 2. Clock Feedthrough

V _S	CLOCK FEEDTHROUGH
5V	400 μ V _{RMS}
\pm 5V	850 μ V _{RMS}

Any parasitic switching transients during the rising and falling edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough can be reduced by adding a single RC lowpass filter at the output (Pin 8) of the LTC1069-7.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and determines the operating signal-to-noise ratio. Most of the wideband noise frequency contents lie within the filter passband. The wideband noise cannot be reduced by adding post filtering. The total wideband noise is nearly independent of

the clock frequency and depends slightly on the power supply voltage (see Table 3). The clock feedthrough specifications are not part of the wideband noise.

Table 3. Wideband Noise

V _S	WIDEBAND NOISE
4.75V	125 μ V _{RMS}
\pm 5V	140 μ V _{RMS}

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs for input frequencies approaching the sampling frequency. The internal sampling frequency of the LTC1069-7 is 50 times its f_{CUTOFF} frequency. For instance if a 48kHz, 100mV_{RMS} signal is applied at the input of an LTC1069-7 operating with a 50% duty cycle 25kHz clock, a 2kHz, 741 μ V_{RMS} alias signal will appear at the filter output. Table 4 shows details.

Table 4. Aliasing

INPUT FREQUENCY V _{IN} = 1V _{RMS}	OUTPUT LEVEL Relative to Input	OUTPUT FREQUENCY Aliased Frequency
$f_{CLK}/f_C = 25:1$, $f_{CUTOFF} = 1\text{kHz}$		
40kHz (or 60kHz)	-59.9dB	10kHz
47kHz (or 53kHz)	-54.2dB	3kHz
48kHz (or 52kHz)	-42.6dB	2kHz
48.5kHz (or 51.5kHz)	-18.3dB	1.5kHz
49kHz (or 52kHz)	-2.9dB	1.0kHz
49.5kHz (or 50.5kHz)	-0.65dB	0.5kHz

Speed Limitations

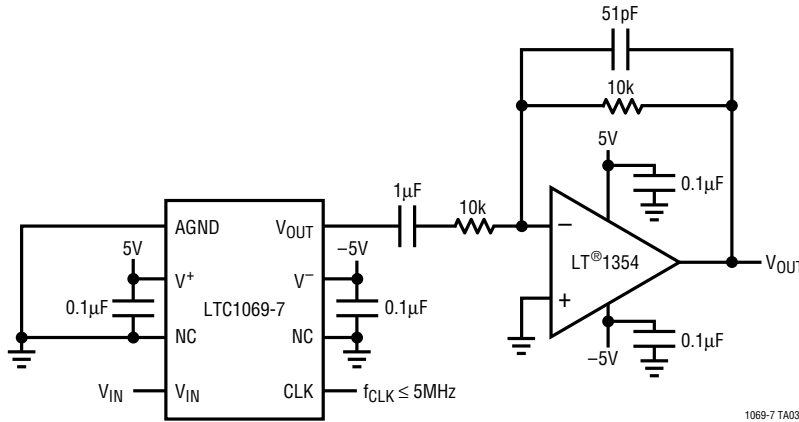
To avoid op amp slew rate limiting, the signal amplitude should be kept below a specified level as shown in Table 5.

Table 5. Maximum V_{IN} vs V_S and Clock

V _S	MAXIMUM CLOCK	MAXIMUM V _{IN}
5V	$\geq 2.5\text{MHz}$	340mV _{RMS} ($f_{IN} \geq 200\text{kHz}$)
$\pm 5\text{V}$	$\geq 4.5\text{MHz}$	1.2V _{RMS} ($f_{IN} \geq 400\text{kHz}$)

TYPICAL APPLICATION

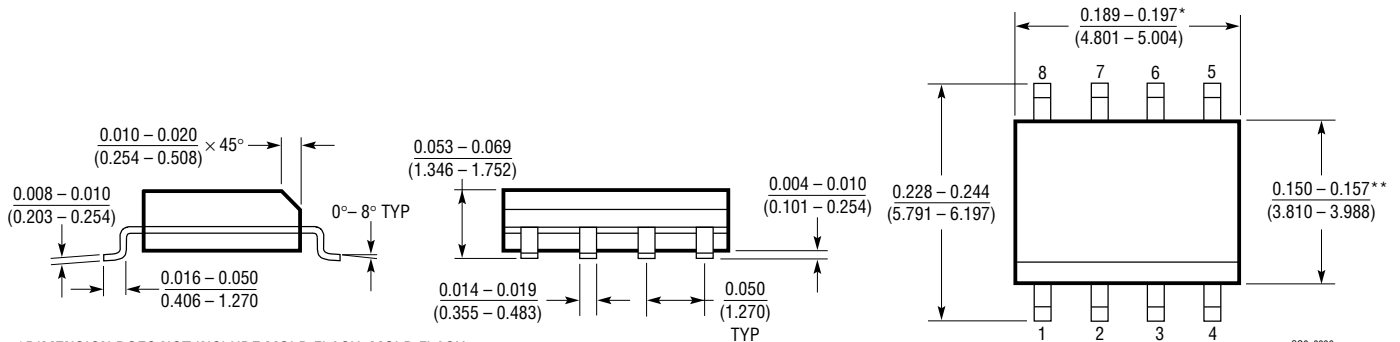
Clock Tunable, Noninverting, Linear Phase 8th Order Filter to 200kHz f_{CUTOFF}



1069-7 TA03

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1064-3	Linear Phase, Bessel 8th Order Filter	$f_{CLK}/f_C = 75/1$ or $150/1$, Very Low Noise
LTC1064-7	Linear Phase, 8th Order Lowpass Filter	$f_{CLK}/f_C = 50/1$ or $100/1$, $f_{C(MAX)} = 100kHz$
LTC1164-7	Low Power, Linear Phase Lowpass Filter	$f_{CLK}/f_C = 50/1$ or $100/1$, $I_S = 2.5mA$, $V_S = 5V$
LTC1264-7	Linear Phase 8th Order Lowpass Filter	$f_{CLK}/f_C = 25/1$ or $50/1$, $f_{C(MAX)} = 200kHz$